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(54) [Title of the Invention] Liquid Crystal Display Device

(57) [Abstract]

[Object] To achieve a liquid crystal display device with high image quality being superior in

insulating film, a reference numeral 134 denotes a silicon layer without an impurity doped, and a reference numeral 135 denotes a silicon layer with an impurity doped.

[0003] Since this sample-hold capacitor is formed of a MOS-type capacitor having the same structure as that of the analog switch TFT, it is possible to increase the capacity per unit area without complicating the manufacturing process and to achieve the capacitor of high throughput while saving the space.

[0004]

[Problem to be solved by the invention] However, when the image of high quality is displayed with high contrast and high resolution, the structure shown in FIG. 9 has the following problem. That is, when an image is displayed with high contrast, it is necessary to form a large sample-hold capacitor in order to decrease a switching noise of the TFT. On the other hand, when an image is displayed with high resolution while keeping the high throughput, it is necessary to increase the number of pixels by narrowing the pixel pitch without changing the chip size and the thickness of the gate insulating film. Therefore, it is required that the sample-hold capacitor is formed to be elongated. In this case, the resistance of the diffusion layer and the poly-silicon gate wiring of the sample-hold capacitor becomes high, which causes a problem that the video signal is not transferred to the sample-hold capacitor sufficiently while the switch TFT is on.

[0005] The present invention is made to solve this problem, and it is an object of the present invention to provide a liquid crystal display device with high image quality being superior in speed of response by forming a low-resistance sample-hold capacitor.

[0006]

[Means to solve the problem] A liquid crystal display device of the present invention is characterized in that a driver circuit for driving a data line is provided with a scanning circuit including a thin film transistor and a sample-hold circuit including a thin film transistor and a MOS-type capacitor of the same structure as that of the thin film transistor and that at least one of a diffusion layer or a gate in the MOS type capacitor is connected in parallel with a wiring having lower resistance than that.

[0007] The liquid crystal display device of the present invention is preferable because a

speed of response.

[Constitution] A liquid crystal display device building-in a driver circuit including a TFT in which a low-resistance wiring is connected in parallel with at least one of a diffusion layer or a gate wiring in a MOS-type hold capacitor of a circuit that samples and holds a video signal.

[Scope of Claim]

[Claim 1] A liquid crystal display device characterized in that a liquid crystal is driven by a group of scanning lines, a group of data lines, a driver circuit for driving the scanning lines and the data lines, and an array of thin film transistors each of which is provided at one of intersections of the scanning lines and the data lines, wherein the driver circuit for driving the data lines is provided with a scanning circuit including a thin film transistor and a sample-hold circuit including a thin film transistor and a MOS-type capacitor having the same structure as that of the thin film transistor, and wherein at least one of a diffusion layer or a gate in the MOS type capacitor is connected in parallel with a wiring having lower resistance than that.

[Detailed description of the invention]

[0001]

[Field of the invention] The present invention relates to a liquid crystal display device including a thin film transistor (hereinafter abbreviated to TFT) and particularly relates to an active matrix panel building-in a driver circuit.

[0002]

[Prior Art] A conventional liquid crystal display device had a structure as shown in FIG. 9 as a sample-hold circuit of the liquid crystal display device building-in the driver circuit as shown in Japanese patent Application laid-open No. 62-178296. In this figure, a reference numeral 131 denotes an analog switch TFT driven by a driver circuit to transfer a video signal to a sample-hold capacitor, a reference numeral 132 denotes a gate wiring made of poly-silicon for forming the sample-hold capacitor, a reference numeral 133 denotes a gate

liquid crystal element, a circuit for driving the liquid crystal, and the other peripheral driver circuits can be formed simultaneously over the same substrate by using a semiconductor substrate having a single-crystal Si layer manufactured by the method hereinafter shown. The method is hereinafter explained.

[0008] The single-crystal Si layer of the semiconductor substrate is formed using a porous Si base substance made in such a way that a single-crystal Si base substance is made porous.

[0009] According to the examination under a transmission electron microscope, the porous Si base substance has pores each of which has a diameter of approximately 600Å on average. Although the density of the porous Si base substance is a half or less of that of the single crystal Si, the single-crystallinity is maintained, and it is possible to grow the single-crystal Si layer epitaxially toward the upper portion of the porous layer. However, at a temperature of 1000 °C or higher, the inside pores are rearranged and the characteristic of the accelerated etching deteriorates. For this reason, low-temperature growth such as a molecular beam epitaxial growth method, a plasma CVD method, a thermal CVD method, a photo CVD method, a bias sputter method, or a liquid crystal growth method is preferable to grow the Si layer epitaxially.

[0010] Here, a method is explained in which after making P-type Si porous, the single-crystal layer is grown epitaxially.

[0011] First, a Si single-crystal base substance is prepared, and it is made porous by an anodization method with the use of an HF solution. Although the density of the single-crystal Si is 2.33 g/cm^3, the density of the porous Si base substance can be changed to be in the range of 0.6 to 1.1 g/cm^3 by changing the concentration of the HF solution to be in the range of 20 to 50 wt%. This porous layer is easily formed in the P-type Si base substance according to the following reason.

[0012] The porous Si is found in the research process of electropolishing of a semiconductor. In the dissolving reaction of Si in the anodization, a hole is necessary for the anodic reaction of Si in the HF solution, which is expressed as follows.

[0013] $Si+2HF+(2-n)e^+ \rightarrow SiF_2+2H^++ne^-$

$SiF_2+2HF \rightarrow SiF_4+H_2$

$SiF_4+2HF \rightarrow H_2SiF_6$

or

$Si+4HF+(4-\lambda)e^+ \rightarrow SiF_4+4H^++\lambda e^-$

$SiF_4+2HF \rightarrow H_2SiF_6$

where e^+ and e^- mean the hole and the electron respectively, and n and λ are the number of holes required to dissolve a Si atom respectively. The porous Si is formed when $n>2$ or $\lambda>4$.

[0014] Thus, it can be said that the P-type Si in which the hole exists is easily made porous.

[0015] On the other hand, it is reported that high-density N-type Si can be also made porous. Therefore, Si can be made porous not depending on the P-type or N-type.

[0016] Since a large number of air spaces are formed inside the porous layer, the density decreases to be a half or less. As a result, since the superficial area increases to a large degree compared with the volume, the chemical etching rate increases remarkably compared with the etching rate of the normal single-crystal layer.

[0017] The condition in order to make the single crystal Si porous by the anodization is shown below. It is noted that the starting material of the porous Si formed by the anodization is not limited to the single-crystal Si, and it may be Si having another crystal structure.

[0018] Applied voltage: 2.6 (V)

Current density: 30 ($mA \cdot cm^{-2}$)

Anodization solution: HF: H_2O: C_2H_5OH=1: 1: 1

Time: 2.4 (hour)

Thickness of the porous Si: 300 (μm)

Porosity: 56 (%)

The single-crystal Si thin film is formed by epitaxially growing Si on the porous Si base substance formed thus. The thickness of the single-crystal Si thin film is preferably 50 μm or less, more preferably 20 μm or less.

[0019] Next, after oxidizing the surface of the above single-crystal Si thin film, a base substance that will constitute a substrate finally is prepared, and then an oxide film on the

surface of the single-crystal Si and the above base substance are pasted. Alternatively, after oxidizing a surface of a single-crystal Si base substance newly prepared, it is pasted to the single-crystal Si layer on the above porous Si base substance. The reason why this oxide film is provided between the base substance and the single-crystal Si layer is as follows. When glass is used as the base substance, for example, the interface state due to the interface of a foundation of the Si active layer can be made lower at the interface of the oxide film than at the interface of the glass. Accordingly, the characteristic of the electronic device can be enhanced considerably. Moreover, only the single-crystal Si thin film with the porous Si base substance etched away by selective etching, which is explained later, may be pasted to the new base substance. They adhere to such a degree that they cannot be parted by means of van der Waals force by pasting them simply in such a way that after their surfaces are washed, they are made to contact each other at the room temperature. Subsequently, this is heated at temperatures from 200 to 900 °C, preferably from 600 to 900 °C, in the nitrogenous atmosphere to paste them completely.

[0020] Furthermore, a Si_3N_4 layer is deposited as an etching prevention film all over the above two base substances to be pasted, and then only the Si_3N_4 layer on the surface of the porous Si base substance is removed. Apiezon Wax may be used instead of the Si_3N_4 layer. After that, the whole porous Si base substance is removed by means of etching or the like, and thus a semiconductor substrate having a thin film single-crystal Si layer is obtained.

[0021] A selective etching method for etching only this porous Si base substance by an electroless wet process is explained.

[0022] As an etchant not having an etching action to crystalline Si but being able to etch only porous Si selectively, a preferable solution is fluorinated acid; buffered fluorinated acid such as ammonium fluoride (NH_4F) or hydrofluoric acid (HF); a mixed solution such as fluorinated acid or buffered fluorinated acid each of which is added with hydrogen peroxide water; a mixed solution such as fluorinated acid or buffered fluorinated acid each of which is added with alcohol; or a mixed solution such as fluorinated acid or buffered fluorinated acid each of which is added with both the hydrogen peroxide water and the alcohol. The etching is performed in such a way that the pasted substrate is moistened by any one of

these solutions. The etching rate depends on the temperature and the concentration of the fluorinated acid solution, the buffered fluorinated acid solution, or the hydrogen peroxide water. Adding the hydrogen peroxide water can accelerate the oxidizing of Si and increase the reaction speed compared with the case not adding the hydrogen peroxide solution. Moreover, the reaction speed can be controlled by changing the proportion of the hydrogen peroxide water. Furthermore, adding the alcohol can remove a bubble of reaction gas formed due to the etching from the etching surface instantaneously without agitating and can etch the porous Si efficiently and homogeneously.

[0023] The concentration of HF in the buffered fluorinated acid with respect to the etchant is preferably from 1 to 95 wt%, more preferably from 1 to 85 wt%, and much more preferably from 1 to 70 wt%. The concentration of NH_4F in the buffered fluorinated acid to the etchant is preferably from 1 to 95 wt%, more preferably from 5 to 90 wt%, and much more preferably from 5 to 80 wt%.

[0024] The concentration of HF to the etchant is preferably from 1 to 95 wt%, more preferably from 5 to 90 wt%, and much more preferably from 5 to 80 wt%.

[0025] The concentration of H_2O_2 to the etchant is preferably from 1 to 95 wt%, more preferably from 5 to 90 wt%, and much more preferably from 10 to 80 wt% within the range where the hydrogen peroxide water works effectively.

[0026] The concentration of the alcohol to the etchant is preferably 80 wt%, more preferably 60 wt% or less, and much more preferably 40 wt% or less within the range where the alcohol works effectively

[0027] The temperature is preferably from 0 to 100 °C, more preferably from 5 to 80 °C, and much more preferably from 5 to 60 °C.

[0028] The alcohol to be used in this process may be ethyl alcohol or may be another alcohol such as isopropyl alcohol that does not cause a practical problem in the manufacturing process and that provides the above-mentioned advantage obtained by adding the alcohol.

[0029] The single-crystal Si layer that is equivalent to a general Si wafer is formed in a large area on the whole substrate obtained thus in such a way that the single-crystal Si layer

is thinned evenly and uniformly.

[0030] The single-crystal Si layer of this semiconductor substrate is separated by a partially oxidizing method or by etching it into an island-shape, and then an impurity is doped therein. Thus, a p or n channel transistor is formed

[0031]

[Operation] According to the above structure of the present invention, it is possible to lower the resistance of the sample-hold capacitor formed to be elongate. Thus, a liquid crystal display device with high image quality of high contrast and high resolution being superior in speed of response can be achieved.

[0032]

[Embodiments]

(Embodiment 1) FIGS. 1 to 3 show a liquid crystal display device in the present embodiment.

[0033] FIG. 1 is an equivalent circuit diagram of the liquid crystal display device in the present embodiment. In this figure, a reference numeral 1 denotes a scanning circuit including a TFT for driving a group of data lines, a reference numeral 2 denotes a video signal line to which a video signal is applied, a reference numeral 3 denotes an output line of the scanning circuit 1 for switching an analog switch TFT 4, a reference numeral 4 denotes the analog switch TFT for transferring the video signal to a MOS-type sample-hold capacitor 6, a reference numeral 5 denotes a wiring for connecting in parallel aluminum and a poly-silicon gate for forming the MOS-type sample-hold capacitor 6, a reference numeral 6 denotes the MOS-type sample-hold capacitor having the same structure as that of the analog switch TFT 4, a reference numeral 7 denotes a wiring for connecting in parallel aluminum and a diffusion layer for forming the MOS-type sample-hold capacitor 6, a reference numeral 8 denotes a constant potential line for supplying a constant potential to the MOS-type sample-hold capacitor 6, a reference numeral 9 denotes a transfer switch TFT for transferring the video signal stored in the MOS-type sample-hold capacitor 6 to a data line 11 and a liquid crystal cell 15, a reference numeral 10 denotes a wiring for switching the transfer switch TFT 9, a reference numeral 11 denotes the data line, a reference numeral

12 denotes a scanning circuit for driving a group of gate lines 13, a reference numeral 14 denotes a pixel switch TFT for writing a signal in the liquid crystal cell 15 of each pixel, a reference numeral 15 denotes the liquid crystal cell, and a reference numeral 16 denotes an opposing electrode.

[0034] FIG. 2 is a plane structure diagram of the MOS-type sample-hold capacitor 6 of the liquid crystal display device of this embodiment. In this figure, a reference numeral 21 denotes a poly-silicon gate for forming the MOS-type sample-hold capacitor, a reference numeral 22 denotes Al connected in parallel with the poly-silicon gate 21, a reference numeral 23 denotes a contact hole for connecting the poly-silicon gate 21 and the Al 22, a reference numeral 24 denotes a diffusion layer for forming the MOS-type sample-hold capacitor, a reference numeral 25 denotes Al connected in parallel with the diffusion layer 24, and a reference numeral 26 denotes a contact hole for connecting the diffusion layer 24 and the Al 25.

[0035] FIG. 3 is a cross-sectional structure diagram corresponding to a position of an extended line of A-A' of FIG. 2 and shows the analog switch TFT 4 and the MOS-type sample-hold capacitor 6 of the liquid crystal display device of this embodiment. In this figure, a reference numeral 31 denotes a silicon substrate, a reference numeral 32 denotes a silicon oxide film, a reference numeral 33 denotes an oxide film formed locally and selectively (LOCOS), a reference numeral 34 denotes a gate insulating film, a reference numeral 35 denotes an analog switch TFT, a reference numeral 36 denotes a poly-silicon gate for forming the MOS-type sample-hold capacitor, a reference numeral 37 denotes Al for connecting the analog switch TFT 35 and the poly-silicon gate 36, a reference numeral 38 denotes Al connected in parallel with the poly-silicon gate 36, a reference numeral 39 denotes an interlayer insulating film, a reference numeral 40 denotes a contact hole for connecting the poly-silicon gate 36 and the Al 38, a reference numeral 41 denotes a silicon layer as a diffusion layer for forming the MOS-type sample-hold capacitor.

[0036] Next, an operation of the liquid crystal display device of this embodiment is explained with reference to FIG. 1.

[0037] A signal transferred to the video signal line 2 is loaded into the MOS-type

sample-hold capacitor 6 through the analog switch TFT 4 in synchronization with a pulse output from the scanning circuit 1 to the output line 3.

[0038] After the analog switch TFT 4 is on for a certain period, it is turned off.

[0039] Within this period, since the resistance of the MOS-type sample-hold capacitor 6 is low, the signal can be loaded from an end of the capacitor into the other end thereof without attenuating the signal.

[0040] Next, the transfer switch 9 is turned on to output a pulse from the scanning circuit 12 to the gate line 13, and the pixel switch 14 is turned on so that the signal is loaded into the display pixel.

[0041] (Embodiment 2) FIGS. 4 to 6 show a liquid crystal display device in this embodiment.

[0042] FIG. 4 is an equivalent circuit diagram of the liquid crystal display device of this embodiment. In this figure, reference numerals denote the same things as those in FIG. 1 except that a reference numeral 55 denotes a wiring to which aluminum and a diffusion layer for forming a MOS-type sample-hold capacitor 56 are connected in parallel and that a reference numeral 57 denotes a wiring to which aluminum and a poly-silicon gate for forming the MOS-type sample-hold capacitor 56 are connected in parallel.

[0043] FIG. 5 is a plane structure diagram of the MOS-type sample-hold capacitor 56 of the liquid crystal display device of this embodiment. In this figure, a reference numeral 71 denotes a diffusion layer for forming the MOS-type sample-hold capacitor, a reference numeral 72 denotes Al connected in parallel with the diffusion layer 71, a reference numeral 73 denotes a contact hole for connecting the diffusion layer 71 and the Al 72, a reference numeral 74 denotes a poly-silicon gate for forming the MOS-type sample-hold capacitor, a reference numeral 75 denotes Al connected in parallel with the poly-silicon gate 74, and a reference numeral 76 denotes a contact hole for connecting the poly-silicon gate 74 and the Al 75.

[0044] FIG. 6 is a cross-sectional structure diagram of an analog switch TFT 54 and the MOS-type sample-hold capacitor 56 of the liquid crystal display device in this embodiment corresponding to a position of an extended line of A-A' in FIG. 5. In this figure, a

reference numeral 81 denotes a silicon substrate, a reference numeral 82 denotes a silicon oxide film, a reference numeral 83 denotes an oxide film formed locally and selectively (LOCOS), a reference numeral 84 denotes a gate insulating film, a reference numeral 85 denotes an analog switch TFT, a reference numeral 86 denotes a silicon layer as a diffusion layer for forming the MOS-type sample-hold capacitor, a reference numeral 87 denotes a high-density silicon layer for having an ohmic contact, a reference numeral 88 denotes Al for connecting the analog switch TFT 85 and the high-density silicon layer 86, a reference numeral 89 denotes a poly-silicon gate for forming the MOS-type sample-hold capacitor, a reference numeral 90 denotes Al connected in parallel with the poly-silicon gate 89, a reference numeral 91 denotes an interlayer insulating film, and a reference numeral 92 denotes a contact hole for connecting the poly-silicon gate 89 and the Al 90.

[0045] The liquid crystal display device of this embodiment operates in the same way as the Embodiment 1.

[0046] (Embodiment 3) FIG. 7 is a plane structure diagram of a MOS-type sample-hold capacitor of the liquid crystal display device in this embodiment. FIG. 8 is a cross-sectional structure diagram of an analog switch TFT and the MOS-type sample-hold capacitor corresponding to a position of an extended line of A-A' in FIG. 7. It is noted that the equivalent circuit diagram is the same as FIG. 1.

[0047] The difference from the Embodiment 1 is explained with reference to FIG. 8. This embodiment is the same as the Embodiment 1 except that a diffusion layer 121 is a silicide layer of Mo, Ti, W, or the like and that the resistance of the poly-silicon gate 116 is not lowered by an Al wiring.

[0048] Although the MOS-type sample-hold capacitor achieves the characteristic of low resistance in such a way that both the gate wiring and the wiring of the diffusion layer are connected in parallel in the Embodiments 1 and 2, the problem of the conventional example can be improved even when the resistance of one of the gate wiring and the wiring of the diffusion layer is lowered.

[0049] Moreover, in the Embodiments 1 to 3, the characteristic of low resistance is achieved by the parallel connection with the use of the aluminum. However, it is not

limited to the aluminum, and the problem of the conventional example can be improved by connecting in parallel a material having lower resistance than the gate wiring and the wiring of the diffusion layer.

[0050] Although the Embodiments 1 to 3 explained the MOS-type sample-hold capacitor having an enhancement-type structure in which the silicon layer is not doped with the impurity of the same type as that in the diffusion layer, the capacitor may have a depletion MOS-type structure in which the impurity of the same type as that in the diffusion layer is doped, and this is not against the concept of the present invention.

[0051] Moreover, a conductivity type of the diffusion layer of the MOS-type capacitor, which is not limited particularly in the Embodiments 1 to 3, may be an N-type or a P-type. Whichever is chosen, it is not against the concept of the present invention.

[0052]

[Effect of the Invention] The liquid crystal display device of the present invention provides the following remarkable effects.

[0053] Generally, the structure of a gate insulating film of a TFT of a liquid crystal display device is set to approximately 700 Å or more in order to secure enough dielectric withstand voltage of 10 V or more while keeping good performance of the transistor. Here, when the MOS-type sample-hold capacitor of 10 pF is formed in 30 μm wide in order to display the image with high contrast and high resolution, the length of the poly-silicon gate layer is approximately 700 μm or more, and its resistance is approximately 1 KΩ or more. Moreover, the resistance of the diffusion layer below the MOS-type sample-hold capacitor is approximately 1 KΩ or more in the same way. In this case, a response frequency of approximately 10 MHz or more is required. However, the response frequency to be obtained actually is approximately 5 MHz or less, and the image signal cannot be transferred to the MOS-type sample-hold capacitor sufficiently. As a result, the image quality deteriorates remarkably.

[0054] When the poly-silicon gate and the diffusion layer are wired in parallel by aluminum according to the present invention, the resistance of those decreases by approximately 3 digits, and the image signal can be transferred to the MOS-type

sample-hold capacitor sufficiently. As a result, the image can be displayed with high contrast and high resolution.

[0055] As thus described, the resistance of the MOS-type sample-hold capacitor can be decreased according to the present invention. Therefore, the liquid crystal display device with high image quality of high contrast and high resolution being superior in speed of response can be achieved.

[Brief description of the drawings]

[FIG. 1] the equivalent circuit diagram of the liquid crystal display device of the Embodiment 1.

[FIG. 2] the plane structure diagram of the MOS-type sample-hold capacitor of the liquid crystal display device of the Embodiment 1.

[FIG. 3] the cross-sectional structure diagram of the analog switch TFT and the MOS sample-hold capacitor of the liquid crystal display device of the Embodiment 1.

[FIG. 4] the equivalent circuit diagram of the liquid crystal display device of the Embodiment 2.

[FIG. 5] the plane structure diagram of the MOS-type sample-hold capacitor of the liquid crystal display device of the Embodiment 2.

[FIG. 6] the cross-sectional structure diagram of the analog switch TFT and the MOS-type sample-hold capacitor of the liquid crystal display device of the Embodiment 2.

[FIG. 7] the plane structure diagram of the MOS-type sample-hold capacitor of the liquid crystal display device of the Embodiment 3.

[FIG. 8] the cross-sectional structure diagram of the analog switch TFT and the MOS-type sample-hold capacitor of the liquid crystal display device of the Embodiment 3.

[FIG. 9] the cross-sectional diagram for explaining the conventional example.